

CLAIMS

What is claimed is:

1. A circuit comprising:
 - a plurality of programmable analog circuit blocks configured to
 - 5 provide at least one of a plurality of analog functions;
 - a plurality of programmable digital circuit blocks configured to
 - provide at least one of a plurality of digital functions;
 - a routing matrix configured to couple a subset of said plurality of
 - programmable analog circuit blocks to a first subset of said plurality of
 - 10 programmable digital circuit blocks, at least a first one of said programmable
 - analog circuit blocks being coupled to at least a first one of said programmable
 - digital circuit blocks, and
 - a programmable interconnect structure comprising said routing
 - matrix and a bus independent of said routing matrix coupling said routing matrix
 - 15 to said plurality of programmable analog circuit blocks and said plurality of
 - programmable digital circuit blocks.
2. A circuit according to Claim 1 wherein said plurality of digital
- functions includes logical operations.
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3. A circuit according to Claim 1 wherein said plurality of digital
- functions includes computational operations.

4. A circuit according to Claim 1 wherein flash memory used to program said programmable interconnect structure and said plurality of programmable analog circuit blocks and said plurality of programmable digital circuit blocks allows for dynamic circuit reconfiguration.

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5. A circuit according to Claim 1 wherein said programmable interconnect structure and said plurality of programmable analog circuit blocks and said plurality of programmable digital circuit blocks are constructed on a semiconductor chip.

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6. A circuit according to Claim 1 wherein said programmable analog circuit blocks may include at least one continuous time analog circuit and at least one switched capacitor analog circuit.

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7. A circuit according to Claim 1 wherein said programmable digital circuit blocks may include at least one standard digital multi-function circuit having a first set of digital functions and at least one enhanced digital multi-function circuit having at least one function differing from said first set of digital functions.

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8. A circuit according to Claim 6 wherein said programmable analog circuit blocks may contain at least one multi-function circuit programmable for at least one of said plurality of analog functions and at least one fixed function

circuit programmable for said fixed function with at least one of a number of different parameters.

9. A microcontroller comprising:

5 a programmable interconnect structure coupling a routing matrix to a plurality of programmable analog circuit blocks and a plurality of programmable digital circuit blocks by means of a bus independent of said routing matrix;

at least a first one of said plurality of programmable analog circuit blocks configurable to provide at least one of a plurality of analog functions, and

10 at least a first one of said plurality of programmable digital circuit blocks configurable to provide at least one of a plurality of digital functions.

10. A circuit according to Claim 9 wherein said plurality of digital functions includes logical operations.

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11. A circuit according to Claim 9 wherein said plurality of digital functions includes computational operations.

12. A circuit according to Claim 9 wherein flash memory used to
20 program said programmable interconnect structure and said plurality of programmable analog circuit blocks and said plurality of programmable digital circuit blocks allows for dynamic circuit reconfiguration.

13. A circuit according to Claim 9 wherein said programmable interconnect structure and said plurality of programmable analog circuit blocks and said plurality of programmable digital circuit blocks are constructed on a semiconductor chip.

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14. A circuit according to Claim 9 wherein said programmable analog circuit blocks may include at least one continuous time analog circuit and at least one switched capacitor analog circuit.

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15. A circuit according to Claim 9 wherein said programmable digital circuit blocks may include at least one standard digital multi-function circuit having a first set of digital functions and at least one enhanced digital multi-function circuit having at least one function differing from said first set of digital functions.

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16. A circuit according to Claim 14 wherein said programmable analog circuit blocks may contain at least one multi-function circuit programmable for at least one of said plurality of analog functions and at least one fixed function circuit programmable for said fixed function with at least one of a number of

20 different parameters.

17. A method of providing a dynamically programmable analog/digital communication interface circuit, comprising:

providing a plurality of programmable analog circuit blocks configurable to at least one of a plurality of analog functions,

5 providing a plurality of programmable digital circuit blocks configurable to at least one of a plurality of digital functions,

providing a routing matrix which will couple analog data and digital data between said programmable analog circuit blocks and said programmable digital circuit blocks,

10 providing a bus independent of said routing matrix which will:

couple analog input/output data to said plurality of programmable analog circuit blocks, and

couple digital input/output data to said plurality of programmable digital circuit blocks,

15 whereby said coupling of said analog input/output data and said digital input/output data are controlled by at least one system clock, and

whereby said dynamically programmable analog/digital communication interface circuit is constructed on one semiconductor chip.

20 18. A circuit according to Claim 17 wherein said programmable analog circuit blocks may include at least one continuous time analog circuit and at least one switched capacitor analog circuit.

19. A circuit according to Claim 17 wherein said programmable digital circuit blocks may include at least one standard digital multi-function circuit

having a first set of digital functions and at least one enhanced digital multi-function circuit having at least one function differing from said first set of digital functions.

5 20. A circuit according to Claim 18 wherein said programmable analog circuit blocks may contain at least one multi-function circuit programmable for at least one of said plurality of analog functions and at least one fixed function circuit programmable for said fixed function with at least one of a number of different parameters.

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 21. A circuit according to Claim 18 wherein said dynamic programming of said communication interface circuit is accomplished by means of flash memory.

15 22. A circuit according to Claim 18 wherein said plurality of digital functions includes logical operations.

 23. A circuit according to Claim 18 wherein said plurality of digital functions includes computational operations.

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